

EC04 804(C)

Analog MOS Circuits

Guide line

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Sincere Thanks to
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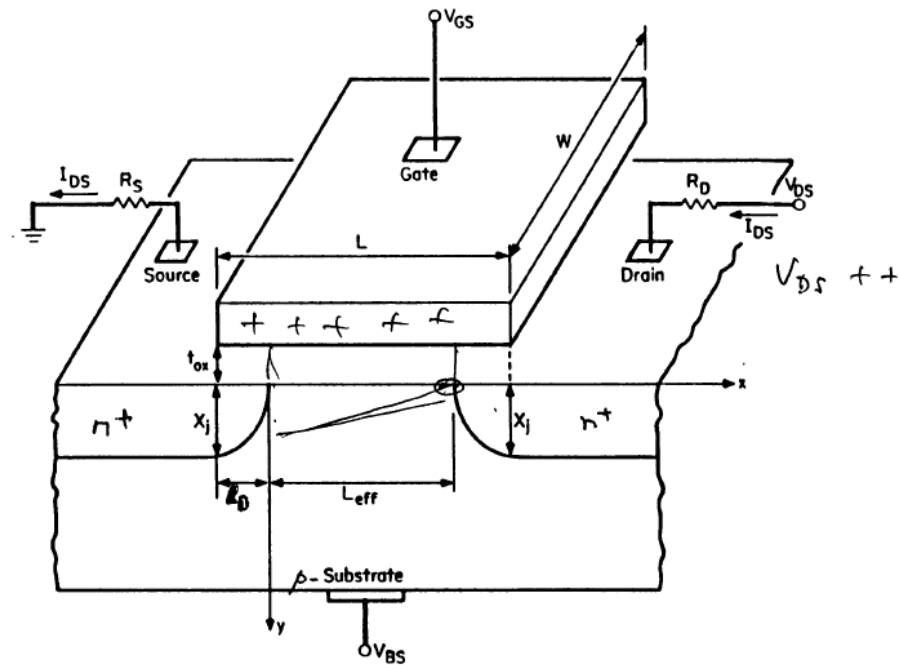
Introduction*

*indicates out of syllabus

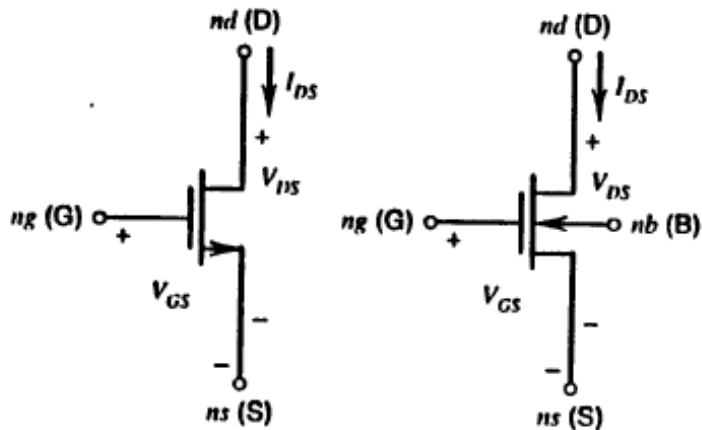
- CMOS circuit design consists of defining i/ps,o/ps hand calculations, ckt simulations, layout of the ckt etc.
- CMOS ICs are fabricated on thin circular slices of Si called wafers. Each wafer contains individual chips or “die”.

Introduction*

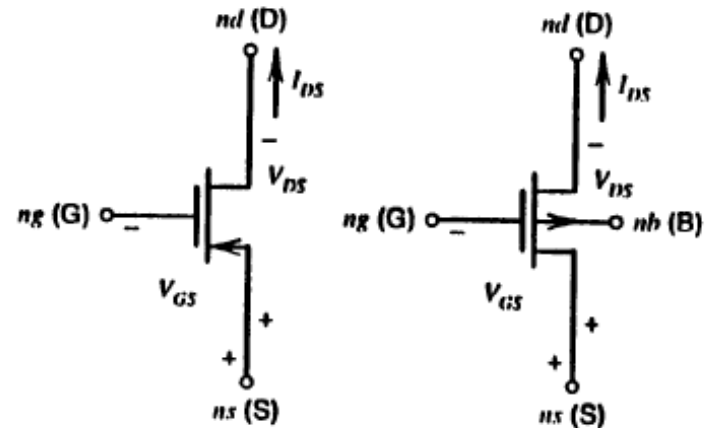
MOSFET



MOSFET symbols*



n-channel



p-channel

MODULE 1

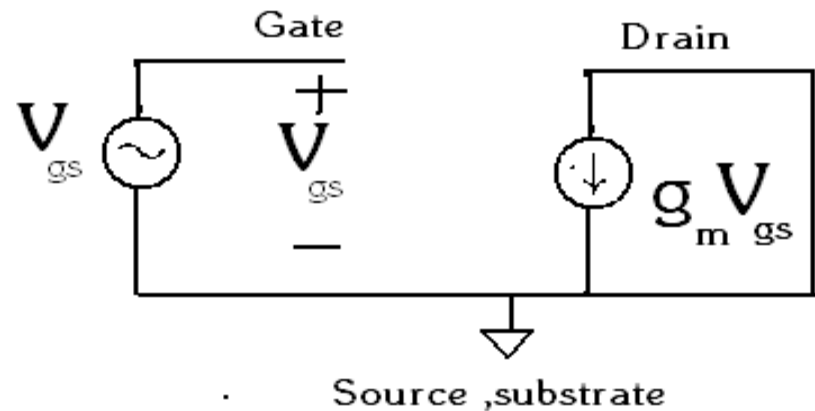
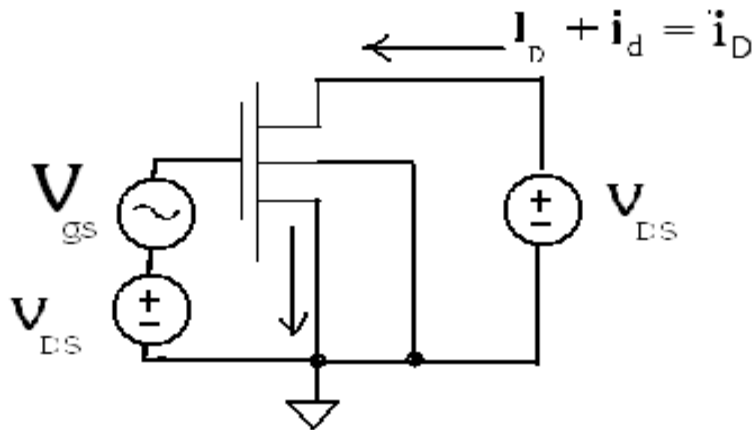
Reference

“CMOS Circuit Design Layout, and
Simulation” Baker, Li, Boyce

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Analog MOS models

- Low frequency model.
 - Study Expressions for Threshold voltage $V_{THN}, I_{D,beta}$
- MOS in saturation (Refer fig9.1 &9.2)
 - When MOSFET is in saturation $V_{DS} > V_{GS} - V_{THN}$



High Frequency Model (Page 171)

- To obtain high frequency model add capacitance to the low frequency model
 - Capacitance b/w gate and Source C_{gs}
 - Capacitance b/w gate and drain C_{gd}
 - Capacitance b/w drain and source diffusion region C_{db}, C_{sb}
 - Capacitance of gate over field region

Temperature effects in MOSFET

- Threshold voltage and Transconductance parameter changes with temperature.

$$\Phi(T) = \frac{\Phi(T_0) T_0}{T} - \frac{3kT \ln(T/T_0)}{q} - \frac{E_g(T_0) T_0}{T} + E_g(T)$$

E_g Silicon Band gap Energy

Noise in MOSFETS

- The noise generators in MOSFETS are due to
 - Thermal noise and
 - Flicker($1/f$ “one over f noise
- The rms thermal noise current is generated by
 - the effective channel resistance($3/2 \cdot 1/g_m$)
 - Parasitic drain, source, gate and substrate resistances (R_D, R_S, R_G, R_B)

Noise in MOST.....

Main motivation for MOS is MODULATION OF RESISTANCE.

TRIODE REGION:
Spectral density,

$$S_{in}(f) = \frac{4KT}{R_{ds}|_{V_{gs}=0}}$$

$$\Rightarrow S_{in}(f) = 4KT\mu C_{ox} \frac{W}{L} (V_{gs} - V_T)$$

SATURATION REGION:
In this region,

$$I_d = f(V_{gs}, V_{ds}) + i_{d,noise}$$

$$\rightarrow S_{in}(f) = \gamma \frac{8}{3} KT g_m$$

$$S_{in}(f) = \gamma \frac{8}{3} KT \mu C_{ox} \frac{W}{L} (V_{gs} - V_T)$$

Noise cont.....

2.2 FLICKER NOISE IN MOS:

Due to impurities @ interface \Rightarrow Flicker noise

Spectral density $\propto \frac{1}{f}$ \Rightarrow Flicker noise is also called $\frac{1}{f}$ noise.

$$S_{\frac{1}{f}}(f) = K_{\frac{1}{f}} \frac{I_d}{L^2} \frac{1}{f}$$

Spectral density

$$S_{\frac{1}{f}}(f) \propto I_d$$

\Rightarrow at $V_{ds} = 0$ there is no flicker noise.

At LOW FREQUENCIES (up to 100MHz) flicker noise dominates.

Module 2

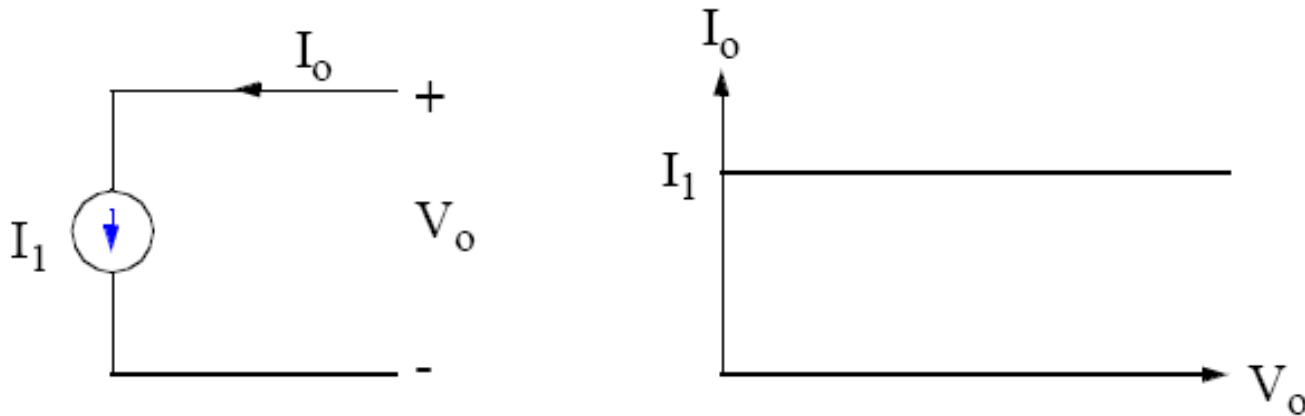
Reference

“CMOS Circuit Design Layout, and
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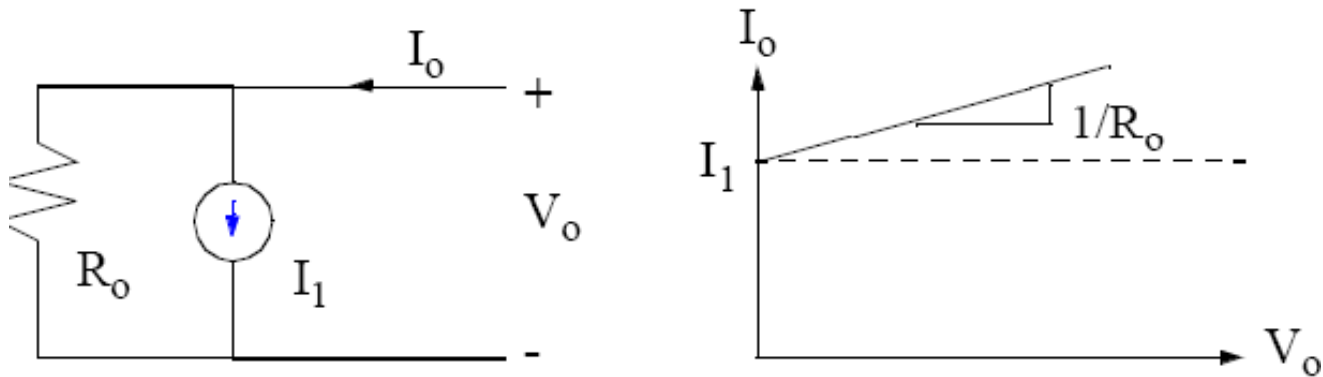
Current sources and Sinks

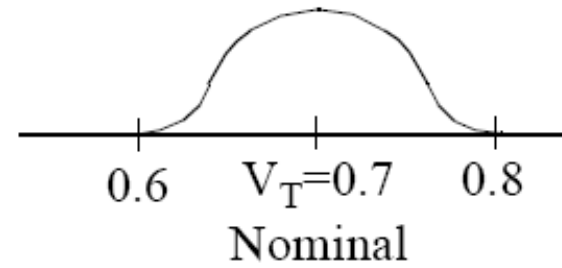
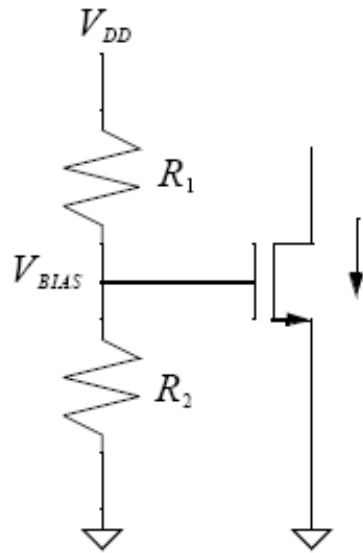
Ideal Current Source



Current sources and Sinks

Real Current Source

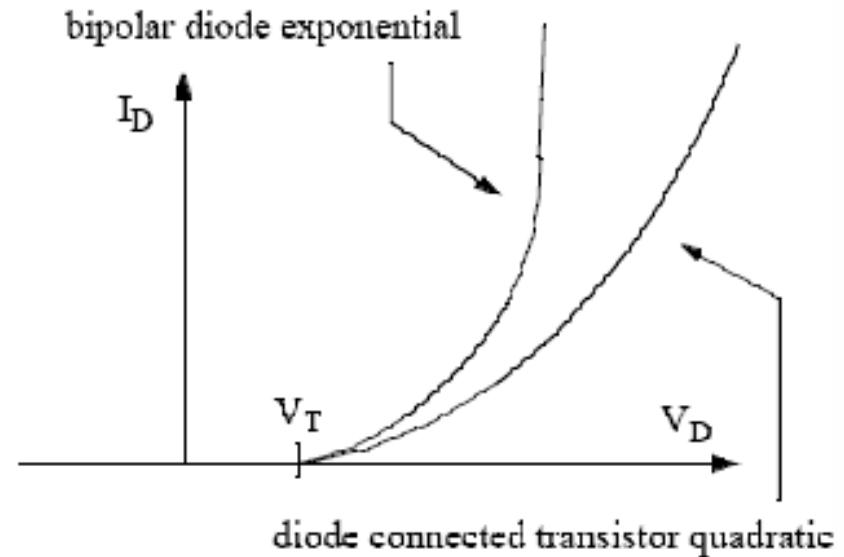
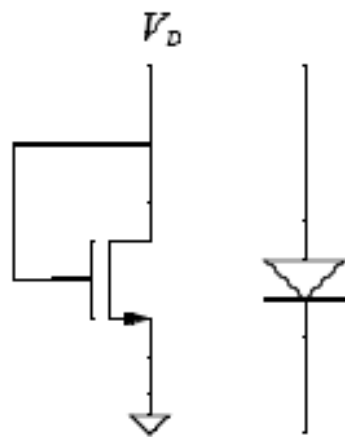




$$I_{DS1} = \frac{W}{L} \cdot \frac{k'}{2} \cdot (V_{BIAS} - V_T)^2$$

Simple source..

Diode Connected Transistor :



$V_{DS} > V_{GS} - V_T$ } After we reach the point $V_D > V_T$, the transistor will always be in Sat.

Simple source..

$$I_{DS1} = \left(\frac{W}{L}\right)_1 \cdot \frac{K'}{2} \cdot (V_{GS1} - V_T)^2$$

$$I_{DS2} = \left(\frac{W}{L}\right)_2 \cdot \frac{K'}{2} \cdot (V_{GS2} - V_T)^2$$

$$\text{if } \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2, \text{ then } I_{DS1} = I_{DS2}$$

$$\text{otherwise } I_{OUT} = I_{REF} \cdot \left[\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} \right]$$

$$I_{REF} = I_{DS1}, \quad I_{OUT} = I_{DS2}$$

Simple source...

Current Calculation :

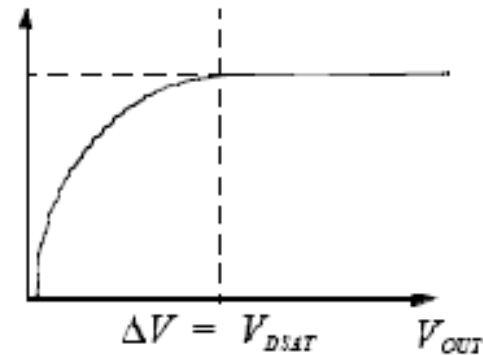
Analysis :

$$I_{DS1} = I_{REF} = \frac{V_{DD} - V_{GS1}}{R_{REF}}$$

$$V_{GS1} = V_T + \left(\frac{2 \cdot I_{DS1}}{k' \cdot \frac{W}{L}} \right)^{\frac{1}{2}} = V_T + \Delta V$$

$$I_{REF} = \frac{V_{DD} - V_T - \left(\frac{2 \cdot I_{REF}}{k' \cdot \frac{W}{L}} \right)^{\frac{1}{2}}}{R_{REF}}$$

Iterative Solution !



Simple source...

Design :

$$R_{REF} = \frac{V_{DD} - V_{GS1}}{I_{REF}} = \frac{V_{DD} - V_T - \left(\frac{2 \cdot I_{REF}}{k' \cdot \frac{W}{L}} \right)^{\frac{1}{2}}}{I_{REF}}$$

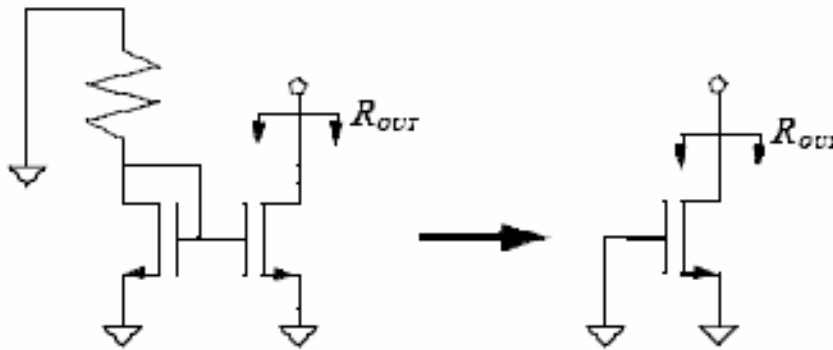
$$I_{REF} = 10 \mu A, V_{DD} = 5, V_T = 0.7$$

$$k' = 90 \times 10^{-6}$$

$$R_{REF} = 415 k\Omega \quad (\text{Pretty Big!})$$

Simple source...

Small Signal:



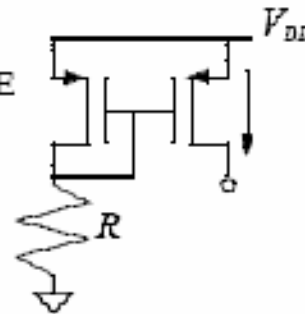
$$R_{out} = r_o = \frac{1}{\lambda \cdot I_{out}}$$

$$I_{out} = 10 \mu A$$

$$\lambda = 0.01$$

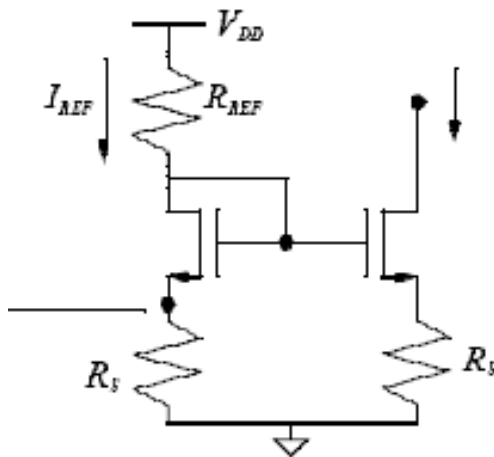
$$R_{out} = 10 M\Omega$$

NMOS → current SINK
PMOS → current SOURCE



Simple source...

How to make R_{OUT} better (ie. larger) ?
Degeneration?



► V_S NOT AT GROUND

$$V_{OUT} > V_{DSAT} + I_{OUT} \cdot R_S$$

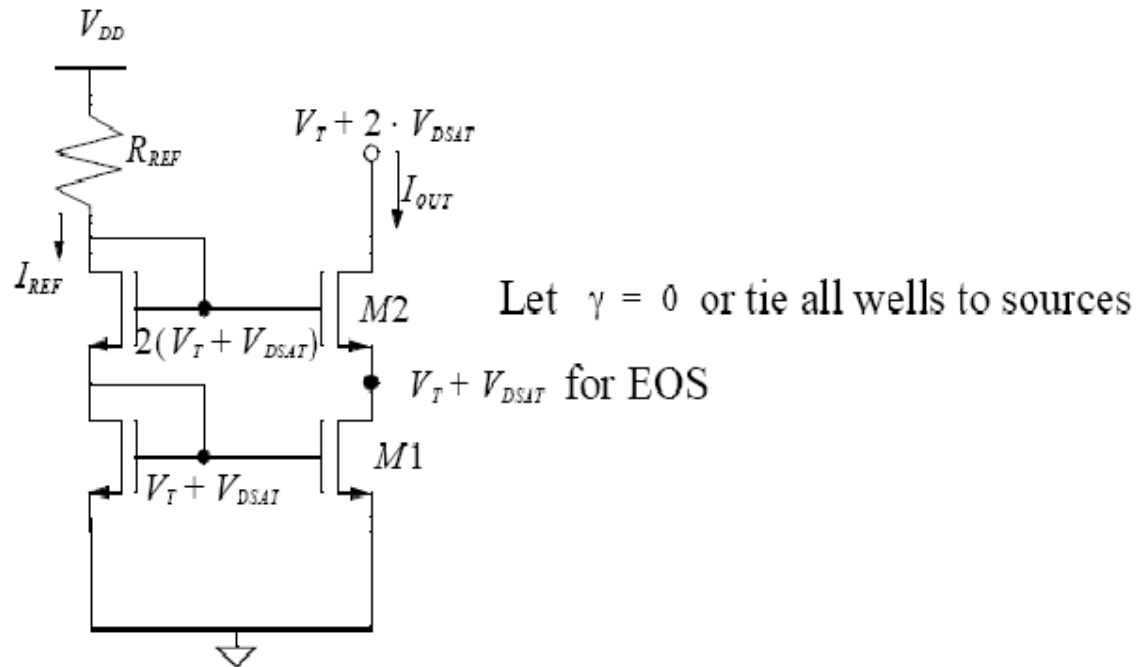
$$R_{OUT} = r_o \cdot [1 + (1 + x) \cdot g_m \cdot R_S]$$

$$V_T = V_{T0} + \gamma \cdot [(V_{SB} + 2 \cdot \phi_f)^{\frac{1}{2}} - (2 \cdot \phi_f)^{\frac{1}{2}}] \quad 7$$

Not a very efficient way to get high R_{OUT} too much area for resistor.
Better method is to use transistors instead of resistors.

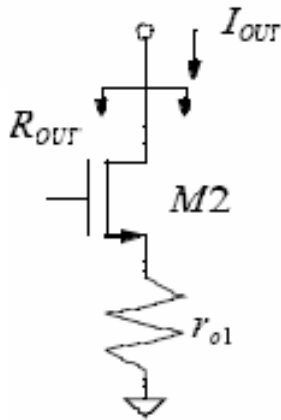
Cascode source

- To increase the output resistance of a current source or sink.



Cascode source

Rout for Cascode Source :



$$\lambda = 0.01$$

$$\gamma = 0$$

$$I_{DS} = 10 \mu A$$

$$\frac{W}{L} = 5$$

$$R_{OUT} = r_{o2} \cdot [1 + (1 + \chi_2) \cdot g_{m2} \cdot r_{o1}]$$

$$\approx (1 + \chi_2) \cdot g_{m2} \cdot r_{o1} \cdot r_{o2}$$

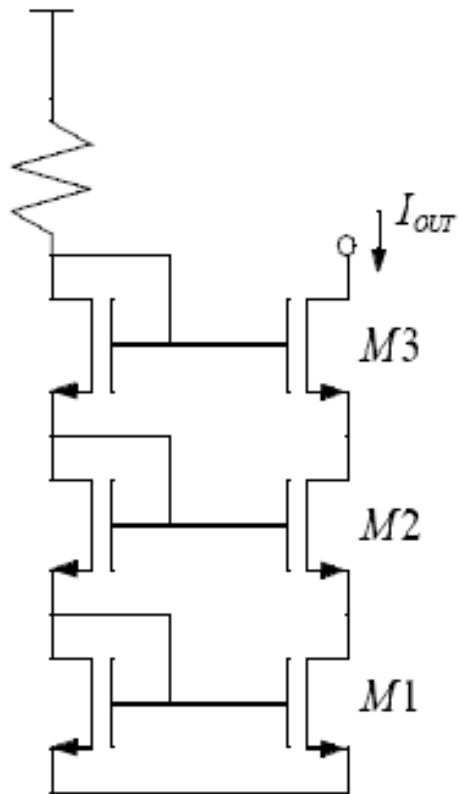
$$r_o = \frac{1}{\lambda \cdot I_{DS}} \quad g_{m2} = \left(2 \cdot k' \cdot \frac{W}{L} \cdot I_{DS} \right)^{\frac{1}{2}} \approx 10^{-4}$$

$$R_{OUT} = 10^{-4} \cdot \left(\frac{1}{0.1 \cdot 10^{-5}} \right)^2 = 10^{10} \Omega$$

$$g_{m2} = \frac{2 \cdot I_{OUT}}{V_{DSAT}} \quad V_{DSAT} \approx 0.2V$$

$$R_{OUT} = \frac{(1 + \chi_2)}{\lambda^2} \cdot \frac{2}{(V_{DSAT}) \cdot (I_{OUT})}$$

Triple Cascode



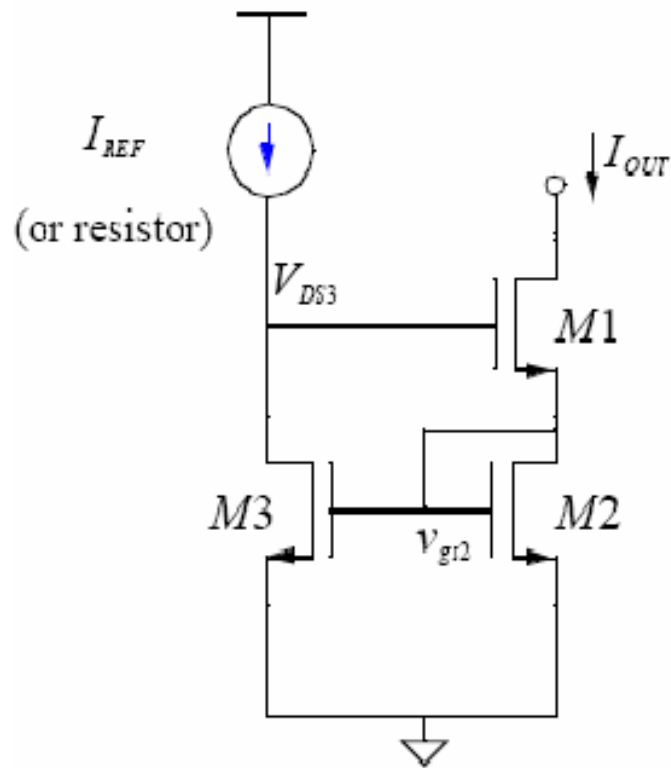
$$R_{OUT} = (1 + \chi_1) \cdot (1 + \chi_3) \cdot g_{m2} \cdot g_{m1} \cdot r_{o1} \cdot r_{o2} \cdot r_{o3}$$

HUGE!!

Other Current sources or Sinks

- The basic current mirror can be improved significantly with negative feedback such as
 - Wilson current mirror
 - Regulated cascode
- Both offer stable current values for wide voltage swings and enhanced output impedance.
- Regulated cascode offer higher degree of o/p impedance & current stability.

Wilson current source



Assume $\gamma = 0$

$$I_{OUT} = I_{REF}$$

$$V_{DS3} = 2 \cdot (V_T + V_{DSAT})$$

Equivalent to Cascode

Regulated cascode

- Regulated cascode Offers significant advantages over others
 1. O/p impedance is significantly higher
 2. Minimum value of V_o is lower than most of the other configurations.
 3. Higher degree of current stability.

References

- In CMOS circuits we derive reference voltages from power supplies by
 - Resistor and MOSFET
 - MOSFET only voltage references
 - Band gap voltage references

Voltage References

- Voltage divider has the advantage of
 - Simplicity
 - Temperature insensitivity
 - Process insensitivity
- But
 - In order to reduce the power dissipation the resistors must be made large. Large resistance require large area in the die → Not practical .

Voltage References

- The voltage divider formed between resistor and MOSFET is the same ckt used for a bias in the current mirror Ref
Page 463
- A MOSFET only Reference is a voltage divider formed between an n and p MOSFETs. It has the advantage that the layout can be small.

Biasing schemes for voltage references

- The resistor-resistor, resistor-MOS, MOS only voltage references are very sensitive to the power supply voltages and temperature.
- So to reduce these the circuits must be properly biased.

Current source self biasing

- **THREE TYPES**
 - Threshold voltage referenced Self –biasing
 - Diode referenced Self Biasing
 - Thermal voltage referenced Self Biasing

Band gap References

- Band gap references combine the +ve Temp Coefficient of the thermal voltage with the –ve Temp Coefficient of the of the diode forward voltage in a circuit to achieve a voltage reference with a zero Temp Coefficient.
- Once we have a temperature independent voltage reference, with the use of an op-amp we can generate multiples of this reference.

to be continued.....