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Chapter 1

ELECTRONIC CIRCUITS LAB

1.1 TRANSISTOR BIASING CIRCUITS

Aim  To bias a given BJT to work in a desired Quiescent operating point by employing different biasing techniques.

Components and equipments required  Transistor, dc source, resistors, bread board, ammeter and voltmeter.

Theory  A BJT must be biased in active operating region to function as an amplifier. In order to bias a BJT in active operating region, base-emitter junction must be forward biased and base-collector junction must be reverse biased. Biasing can be done with the help of a DC source and a few resistors. Different methods are used to bias the BJT. The objective of this experiment is to study the effect of the variation of the parameters on the operating point.

Fixed bias circuit  A resistor is used to tie the base of the transistor to $V_{CC}$ for the fixed bias set up. Saturation conditions are avoided in this bias set up because the base-collector junction is no longer reverse biased. Therefore the signal output will not be distorted. However the stability of the circuit is poor against the parameter variations.

Emitter-stabilized bias circuit  The stability of the fixed bias circuit can be improved significantly by introducing a resistor $R_E$ in the emitter terminal.

Collector feedback bias circuit  Stability can be improved by introducing a feedback path from collector to base through a resistor. Though Q-point is not completely independent of $\beta$ ($h_{FE}$), current gain of the transistor, sensitivity to changes in $\beta$ or temperature variations are less than that for fixed bias and emitter-bias configurations.

Voltage divider bias circuit  A potential divider resistor network $R_1R_2$ provides
the sufficient voltages across the transistor junctions. This amplifier set up is almost
independent of $\beta$. $R_1$ and $R_2$ are designed such that a stable voltage drop exists across
them even when the base current varies. For this, current through $R_1$ and $R_2$ is assumed
to be the same and it is much higher than the base current. Therefore $R_2$ is made much
greater than the resistance across base and emitter which is $(1 + \beta)R_E$. $R_E$ includes
internal emitter resistance $r_e$ also.

**Procedure**

1. Set up the fixed bias circuit after testing the components. Vary only one of the
parameters $V_{CC}$, $R_C$, $R_B$ and $\beta$ and enter the updated values in the table. To
change $\beta$, use transistor BC177 whose $\beta$ is 75.
2. Repeat the experiments by changing other parameters. Draw the load line on a
graph with $V_{CE}$ along x-axis and $I_C$ along y-axis.
3. Set up other bias circuits one by one. Repeat the experiments by changing one
parameter at a time.

**Fixed bias circuit**

![Fixed bias circuit diagram]

<table>
<thead>
<tr>
<th>$V_{CC}$</th>
<th>$R_C$</th>
<th>$R_B$</th>
<th>$\beta$</th>
<th>$V_{CE}$</th>
<th>$I_C$</th>
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</tbody>
</table>

**Design**

Select transistor BC107 since its $\beta$ ranges from 100 to 500 at $I_C = 2$ mA, as per
data sheet.

Let the Q-point be $V_{CE} = 6$ V, and $I_C = 2$ mA at $V_{CC} = 12$ V.

Then $V_{RC} = I_C \times R_C = 6$ V.

From this, $R_C = 3$ k. Use 3.3 k std.
Design

Let the Q-point be $V_{CE} = 6 \text{ V}$, and $I_C = 2 \text{ mA}$ at $V_{CC} = 12 \text{ V}$.

Voltage across $R_C = 6 \text{ V}$. From this, $R_C = 3 \text{ k}$. Use $3.3 \text{ k}$.

$V_{RB} = V_{CE} - V_{BE} = 6 \text{ V} - 0.7 \text{ V} = 5.3 \text{ V}$.

Also, $V_{RB} = I_B \times R_B = 5.3 \text{ V}$. From this, $R_B = 265 \text{ k}$. Use $220 \text{ k}$.

Voltage divider bias

Design

Let the Q-point be $V_{CE} = 6 \text{ V}$, and $I_C = 2 \text{ mA}$ at $V_{CC} = 12 \text{ V}$.

Assume voltage across $R_C = 4 \text{ V}$ and that across $R_E = 2 \text{ V}$.

$V_{RC} = I_C \times R_C = 4 \text{ V}$. From this, we get $R_C = 2 \text{ k}$. Use $2.2 \text{ k std}$.

$V_{RE} = I_E \times R_E = 2 \text{ V}$. Because, $I_E \approx I_C$. From this, we get $R_E = 1 \text{ k}$.

Design of voltage divider $R_1$ and $R_2$

Assume the current through $R_1 = 10I_B$ and that through $R_2 = 9I_B$ to avoid loading of the potential divider network $R_1$ and $R_2$ by the base current. (In other words to keep the bias voltages across $R_1$ and $R_2$ stable against the base current variations).

i.e., $V_{R2} = V_{BE} + V_{RE} = 0.6 \text{ V} + 2 \text{ V} = 2.6 \text{ V}$. Also, $V_{R2} = 9I_BR_2 = 2.6 \text{ V}$

But $I_B = I_C/\beta = 2 \text{ mA/100} = 20 \mu\text{A}$. Then $R_2 = \frac{2.6}{9 \times 20 \times 10^{-6}} = 14 \text{ k}$. Use $15 \text{ k}$.

$V_{R1} = \text{Voltage across } R_1 = V_{CC} - V_{R2} = 12 \text{ V} - 2.6 \text{ V} = 9.4 \text{ V}$

Also, $V_{R1} = 10I_BR_1 = 9.4 \text{ V}$. Then $R_1 = \frac{9.4}{10 \times 20 \times 10^{-6}} = 47 \text{ k}$. 

<table>
<thead>
<tr>
<th>$V_{CC}$</th>
<th>$R_C$</th>
<th>$\beta$</th>
<th>$V_{CE}$</th>
<th>$I_C$</th>
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1.2 RC-COUPLED AMPLIFIER

Aim To design and set up an RC-coupled CE amplifier using bipolar junction transistor and to plot its frequency response.

Components and equipments required Transistor, dc source, capacitors, resistors, bread board, signal generator, multimeter and CRO.

Theory RC-coupled CE amplifier is widely used in audio frequency applications in radio and TV receivers. It provides current, voltage and power gains. Base current controls the collector current of a common emitter amplifier. A small increase in base current results in a relatively large increase in collector current. Similarly, a small decrease in base current causes large decrease in collector current. The emitter-base junction must be forward biased and the collector base junction must be reverse biased for the proper functioning of an amplifier. In the circuit diagram, an NPN transistor is connected as a common emitter ac amplifier. $R_1$ and $R_2$ are employed for the voltage divider bias of the transistor. Voltage divider bias provides good stabilisation independent of the variations of $\beta$. The input signal $V_{in}$ is coupled through $C_{C1}$ to the base and output voltage is coupled from collector through the capacitor $C_{C2}$.

The input impedance of the amplifier is expressed as $Z_{in} = R_1||R_2||(1+h_{FE}r_e)$ and output impedance as $Z_{out} = R_C||R_L$ where $r_e$ is the internal emitter resistance of the transistor given by the expression $= 25 \text{ mV}/I_E$, where 25 mV is temperature equivalent voltage at room temperature.

Selection of transistor Transistor is selected according to the frequency of operation, and power requirements. The $h_{FE}$ of the transistor is another aspect we should be careful about. Low frequency gain of a BJT amplifier is given by the expression.

Voltage gain $A_v = -h_{FE}R_L/R_i$. In the worst case with $R_L = R_i$, $A_v = -h_{FE}$. $h_{FE}$ of any transistor will vary in large ranges. For example, the $h_{FE}$ of SL100 (a general purpose transistor) varies from 40 to 300. $h_{FE}$ of BC107 (an AF driver) varies from 100 to 500. Therefore a transistor must be selected such that its minimum guaranteed $h_{FE}$ is greater than or equal to $A_v$ required.

Selection of supply voltage $V_{CC}$ For a distortionless output from an audio amplifier, the operating point must be kept at the middle of the load line selecting $V_{CEQ} = 50\% V_{CC}(= 0.5V_{CC})$. This means that the output voltage swing in either positive or negative direction is half of $V_{CC}$. However, $V_{CC}$ is selected 20% more than the required voltage swing. For example, if the required output swing is 10 V, $V_{CC}$ is selected 12 V.

Selection of collector current $I_C$ The nominal value of $I_C$ can be selected from
the data sheet. Usually it will be given corresponding to $h_{FE}$ bias. It is the bias current at which $h_{FE}$ is measured. For BC107 it is 2 mA, for SL100 it is 150 mA, and for power transistor 2N3055 it is 4 A.

**Design of emitter resistor $R_E$**  
Current series feedback is used in this circuit using $R_E$. It stabilizes the operating point against temperature variation. Voltage across $R_E$ must be as high as possible. But, higher drop across $R_E$ will reduce the output voltage swing. So, as a rule of thumb, 10% of $V_{CC}$ is fixed across $R_E$.

$$R_E = \frac{V_{RE}}{I_E} = \frac{V_{RE}}{I_C} \quad \text{since} \quad I_E \approx I_C, \quad R_E = 0.1 \frac{V_{CC}}{I_C}$$

**Design of $R_C$**  
Value of $R_C$ can be obtained from the relation $R_C = 0.4V_{CC}/I_C$ since remaining 40% of $V_{CC}$ is dropped across $R_C$.

**Design of potential divider $R_1$ and $R_2$**  
Value of $I_B$ is obtained by using the expression $I_B = I_C/h_{FE}$ min. At least 10$I_B$ should be allowed to flow through $R_1$ and $R_2$ for the better stability of bias voltages. If the current through $R_1$ and $R_2$ is near to $I_B$, slight variation in $I_B$ will affect the voltage across $R_1$ and $R_2$. In other words, the base current will load the voltage divider. When $I_B$ gets branched into the base of transistor, 9$I_B$ flows through $R_2$. Values of $R_1$ and $R_2$ can be calculated from the dc potentials created by the respective currents.

**Design of bypass capacitor $C_E$**  
The purpose of the bypass capacitor is to bypass signal current to ground. To bypass the frequency of interest, reactance of the capacitor $X_{CE}$ computed at that frequency should be much less than the emitter resistance. As a rule of thumb, it is taken $X_{CE} \leq R_E/10$.

**Design of coupling capacitor $C_C$**  
The purpose of the coupling capacitor is to couple the ac signal to the input of the amplifier and block dc. It also determines the lowest frequency that to be amplified. Value of the coupling capacitor $C_C$ is obtained such that its reactance $X_C$ at the lowest frequency (say 100 Hz or so for an audio amplifier), should be less than the input impedance of the amplifier. That means $X_C$ must be $\leq R_{in}/10$. Here $R_{in} = R_1||R_2||(1 + h_{FE}r_e)$ where $r_e$ is the internal emitter resistance of the transistor given by the expression $= 25 \text{ mV}/I_E$ at room temperature.

**Procedure**

1. Test all the components using a multimeter. Set up the circuit and verify dc bias conditions. To check dc bias conditions, remove input signal and capacitors in the circuit.

2. Connect the capacitors in the circuit. Apply a 100 mV peak to peak sinusoidal signal from the function generator to the circuit input. Observe the input and output waveforms on the CRO screen simultaneously.
3. Keep the input voltage constant at 100 mV, vary the frequency of the input signal from 0 to 1 MHz or highest frequency available in the generator. Measure the output amplitude corresponding to different frequencies and enter it in tabular column.

4. Plot the frequency response characteristics on a graph sheet with gain in dB on y-axis and \( \log f \) on x-axis. Mark \( \log f_L \) and \( \log f_H \) corresponding to 3 dB points. (If a semi-log graph sheet is used instead of ordinary graph sheet, mark \( f \) along x-axis instead of \( \log f \)).

5. Calculate the bandwidth of the amplifier using the expression \( \text{BW} = f_H - f_L \).

6. Remove the emitter bypass capacitor \( C_E \) from the circuit and repeat the steps 3 to 5 and observe that the bandwidth increases and gain decreases in the absence of \( C_E \).

**Circuit diagram**

![Circuit diagram of the amplifier](image)

**Design**

Output requirements: Mid-band voltage gain of the amplifier = 50 and required output voltage swing = 10 V.

**Selection of transistor** Select transistor BC107 since its minimum guaranteed \( h_{FE}(= 100) \) is more than the required gain (=50) of the amplifier.

**Quick Reference data of BC107**

Type: NPN-Silicon, Application: In audio frequency
Maximum rating: $V_{CB} = 50 \text{ V}, V_{CE} = 45 \text{ V}, V_{EB} = 6 \text{ V}, I_C = 100 \text{ mA}$.

Nominal rating: $V_{CE} = 5 \text{ V}, I_C = 2 \text{ mA}, h_{FE} = 100$ to 500.

**DC biasing conditions**  $V_{CC}$ is taken as 20% more than required output swing. Hence $V_{CC} = 12 \text{ V}$.

$I_C = 2 \text{ mA}$, because $h_{FE}$ is guaranteed 100 at that current as per data sheet.

In order to make the operating point at the middle of the load line, assume the dc conditions $V_{RC} = 40\%$ of $V_{CC} = 4.8 \text{ V}$, $V_{RE} = 10\%$ of $V_{CC} = 1.2 \text{ V}$ and $V_{CE} = 50\%$ of $V_{CC} = 6 \text{ V}$.

**Design of $R_C$**  $V_{RC} = I_C \times R_C = 4.8 \text{ V}$. From this, we get $R_C = 2.4 \text{ k}$. Use $2.2 \text{ k}$.

**Design of $R_E$**  $V_{RE} = I_E \times R_E = 1.2 \text{ V}$. From this, we get $R_E = 600 \Omega$ because $I_E \approx I_C$. Use $680 \Omega$ std.

**Design of voltage divider $R_1$ and $R_2$**

Assume the current through $R_1 = 10I_B$ and that through $R_2 = 9I_B$ for a stable voltage across $R_1$ and $R_2$ independent of the variations of the base current.

$V_{R_2} = $ Voltage drop across $R_2 = V_{BE} + V_{RE}$.

i.e., $V_{R_2} = V_{BE} + V_{RE} = 0.6 + 1.2 = 1.8 \text{ V}$. Also, $V_{R_2} = 9I_BR_2 = 1.8 \text{ V}$

But $I_B = I_C/h_{FE} = 2 \text{ mA}/100 = 20 \mu\text{A}$. Then $R_2 = \frac{1.8}{9 \times 20 \times 10^{-6}} = 10.6 \Omega$. Use $10 \Omega$.

$V_{R_1} = $ voltage across $R_1 = V_{CC} - V_{R_2} = 12 \text{ V} - 1.8 \text{ V} = 10.2 \text{ V}$

Also, $V_{R_1} = 10I_BR_1 = 10.1 \text{ V}$. Then $R_1 = \frac{10.2}{10 \times 20 \times 10^{-6}} = 50 \text{ k}$. Select $47 \text{ k}$ std.

**Design of $R_L$**: Gain of the common emitter amplifier is given by the expression $A_V = -(r_c/r_e)$. Where $r_c = R_C||R_L$ and $r_c = 25 \text{ mV}/I_E = 25 \text{ mV}/2 \text{ mA} = 12.5 \Omega$.

Since the required gain = 50, substituting it in the expression we get, $R_L = 845 \Omega$. Use $820 \Omega$ std.

**Design of coupling capacitors $C_{C1}$ and $C_{C2}$**

$X_{C1}$ should be less than the input impedance of the transistor. Here, $R_{in}$ is the series impedance.

Then $X_{C1} \leq R_{in}/10$. Here $R_{in} = R_1||R_2||(1 + h_{FE}r_e)$ because is $R_E$ bypassed.

We get $R_{in} = 1.1 \text{ k}$. Then $X_{C1} \leq 110 \Omega$.

So, $C_{C1} \geq 1/2\pi f_L \times 110 = 14 \mu\text{F}$. Use $15 \mu\text{F}$ std.
Similarly, \( X_{C2} \leq R_{out}/10 \), where \( R_{out} = R_C \). Then \( X_{CE} \leq 240 \, \Omega \).

So, \( C_{C2} \geq 1/2\pi \times 240 = 6.6 \, \mu F \). Use 10 \( \mu F \) std.

**Design of bypass capacitors \( C_E \)**

To bypass the lowest frequency (say 100Hz), \( X_{CE} \) should be less than or equal to the resistance \( R_E \).

i.e., \( X_{CE} \leq R_E/10 \) Then, \( C_E \geq 1/(2\pi \times 100 \times 68) = 23 \, \mu F \). Use 22 \( \mu F \).

**Graph**

![Gain in dB graph](image)

**Result**

With \( C_E \):
- Mid-band gain of the amplifier = .......
- Bandwidth of the amplifier = ....... Hz

Without \( C_E \):
- Mid-band gain of the amplifier = .......
- Bandwidth of the amplifier = ....... Hz

**Troubleshooting**

1. Before the ac signal is applied, check dc conditions of the amplifier. Ensure that the transistor is in active region by verifying that the E-B junction is forward biased and C-B junction is reverse biased.

2. Replace \( R_E \) by a pot and connect the bypass capacitor at the variable terminal of the pot. Verify whether \( V_{BE} = 0.6 \, V \). This is very important.

3. If the output waveform gets clipped, reduce the amplitude of the input signal, vary \( R_C \) or adjust \( V_{CC} \) slightly.

4. If the voltage at the collector \( V_C = 12 \, V \), collector circuit is not drawing current. Transistor is in cut off state. Base-emitter junction may not be forward biased.

5. If \( V_C = 0 \), possible trouble is open collector circuit or collector shorted to earth. If \( V_E = 0 \), emitter is drawing current.
Answered examination questions

1. Design and set up an amplifier for the specifications: gain = -50, output voltage = 10 \(V_{PP}\), \(f_L = 50\) Hz and calculate \(Z_i\).

Negative sign of the gain indicates that the output of an \(RC\) coupled amplifier is the amplified and inverted version of the input. \(f_L\) should be considered while designing the coupling capacitor. Set up an \(RC\) coupled amplifier for a gain of 50. To obtain an output voltage of 10 V peak to peak, take \(V_{CC}\) 20\% more than the required voltage swing. i.e., 12 V. To measure the input impedance, connect a 10 \(k\) resistor in series with the function generator and note down the potential difference across the resistor. Then calculate the current through the resistor. The input impedance is equal to the ratio of the voltage at the right side of the 10 \(k\) resistor with respect to the current through it.

2. Set up an \(RC\) coupled amplifier and measure its input and output impedances.

   Measurement of input resistance  
   Method 1: Connect a known resistor (say 1 \(k\)) in series between the signal generator and the input of the circuit. Calculate the current through the resistor from the potential difference across it. Since this current also flows into the circuit, input resistance can be measured taking the ratio of the voltage at the right side of the resistor to the current.

   Method 2: Connect a pot in series between the signal source and the input of the circuit. Adjust the pot until the input voltage to the circuit is 50\% of the signal generator voltage. Remove the pot from the circuit and measure its resistance using a multimeter.

   Measurement of output resistance  
   Method 1: Measure the open circuit output voltage. This is the Thevenin voltage. Output resistance of the circuit is actually the Thevenin resistance in series with the Thevenin voltage. Connect a known value resistor, say 1 \(k\) and measure the voltage across it. A reduction in the output voltage can be observed. Calculate the current through the resistor. Since this current also flows through the Thevenin resistance, output resistance is the ratio of the difference in the output voltage to the current.

   Method 2: Connect a pot at the output of the circuit. Adjust the pot until the voltage across it is 50\% of the open circuit voltage. Remove the pot from the circuit and measure its resistance using a multimeter.

3. Set up an \(RC\) coupled amplifier using a PNP transistor for a gain = 20 dB and stability factor = 5.

   When a PNP transistor is used, polarity of supply voltage \(V_{CC}\) must be reversed. Convert dB to linear scale. Take stability factor \(5 = 1 + R_B/R_E\), where \(R_B = R_1\) parallel with \(R_2\).

4. Design and set up an \(RC\) coupled amplifier for a stability factor of 5 and \(f_H = 30\) kHz.

   Design the amplifier as described in the previous question. Use a capacitor in parallel to the output to function as a low pass filter for a cut off frequency \(f_H = 1/2\pi R_C C\).
11. How is the input of the $RC$ coupled amplifier phase shifted by $180^\circ$ at the output?

The collector voltage is given by the expression $V_C = V_{CC} - I_C R_C$. The increase in the input voltage causes an increase in the collector current. Increase in the collector current reduces the collector voltage. Inverse is also true. Thus the amplifier provides the phase inversion.

Exercise

1. Differentiate between ac and dc load lines? Explain their importance in amplifier analysis.

2. Why is the center point of the active region chosen for dc biasing?

3. What happens if extreme portions of the active region are chosen for dc biasing?

4. Draw the output characteristics of the amplifier and mark the load-line on it. Also mark the three regions of operation on the output characteristics.

5. Which are the different forms of coupling used in multi-stage amplifiers?

6. Draw hybrid and hybrid-$\pi$ equivalent models of a transistor in the $CE$ configuration.

7. Draw the Ebers-Moll model of a BJT.

8. What are self bias and fixed bias?

9. Give a few applications of $RC$-coupled amplifier.

<table>
<thead>
<tr>
<th>Number</th>
<th>Type</th>
<th>Application</th>
<th>$I_C$</th>
<th>$\beta = h_{FE}$</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>BC107</td>
<td>Si, NPN</td>
<td>Audio, low power</td>
<td>100 mA</td>
<td>100-500</td>
<td>TO 18</td>
</tr>
<tr>
<td>2N2222</td>
<td>Si, NPN</td>
<td>Switching</td>
<td>800 mA</td>
<td>100-300</td>
<td>TO 18</td>
</tr>
<tr>
<td>SL100</td>
<td>Si, NPN</td>
<td>General purpose</td>
<td>1 A</td>
<td>40-300</td>
<td>TO 5</td>
</tr>
<tr>
<td>SK100</td>
<td>Si, PNP</td>
<td>General purpose</td>
<td>1 A</td>
<td>40-300</td>
<td>TO 5</td>
</tr>
<tr>
<td>BC147</td>
<td>Si, NPN</td>
<td>Driver</td>
<td>200 mA</td>
<td>125-500</td>
<td>MM 10</td>
</tr>
<tr>
<td>BC177</td>
<td>Si, PNP</td>
<td>Driver</td>
<td>200 mA</td>
<td>75-260</td>
<td>TO 18</td>
</tr>
<tr>
<td>BF194</td>
<td>Si, NPN</td>
<td>AM radio</td>
<td>30 mA</td>
<td>67-220</td>
<td>TO 92</td>
</tr>
<tr>
<td>BF195</td>
<td>Si, NPN</td>
<td>AM radio</td>
<td>30 mA</td>
<td>36-125</td>
<td>MM 10</td>
</tr>
<tr>
<td>2N3055</td>
<td>Si, NPN</td>
<td>High power</td>
<td>15 A</td>
<td>20-70</td>
<td>TO 3</td>
</tr>
</tbody>
</table>
1.3 TWO STAGE RC-COUPLED AMPLIFIER

Aim To design, set up and study a two stage RC coupled CE amplifier using BJT.

Components and equipments required Transistor, dc source, capacitors, resistors, bread board, signal generator, multimeter and CRO.

Theory Multistage amplifiers are used in cascade to improve parameters such as voltage gain, current gain, input impedance and output impedance etc. Common emitter stages are cascaded to increase the voltage gain. A two stage amplifier provides an overall voltage gain of $A_1A_2$, where $A_1$ and $A_2$ are the gains of first and second stages respectively. Since each stage provides a phase inversion, the final output signal is in phase with the input signal.

The input impedance of the second stage is in parallel with $R_{C1}$ of the first stage. The ac voltage gain of the first stage is $A_1 = R_{C1}|R_{in2}/(r_e + R_e)$ where $R_{in2}$ is the input resistance of the second stage. $R_{in2} = R_{12}|R_{22}|(1 + h_{FE}r_e)$

The ac voltage gain of the second stage is $A_2 = (R_{C2}|R_{L})/r_e$

Care must be taken while selecting $A_1$ and $A_2$. If $A_1$ is large, the input to the second stage will become too high. This may pull out the transistor of the second stage from active region. For example, if we need an overall voltage gain of 100, select $A_1 = 4$ and $A_2 = 25$. Gain of the first stage can be controlled by a negative feed back in series with the emitter. This is achieved by the unbypassed resistor $R_e$.

Circuit diagram
\( R_L C_C >> T_S \) where \( T_S \) is the lowest signal frequency (20 Hz).

\[ C_C = \frac{1}{(2\pi 20 R_L)} = 360 \, \mu F. \] Use 470 \( \mu F \) std.

**Class-AB power amplifier**

![Class-AB power amplifier circuit diagram]

**Design**

**Design of class-AB power** Design of \( R_L \) and \( C_C \) is same as that of class-B amplifier.

**Design of \( R \) and \( R_B \)** The bias current through the compensating diodes \( I_D \) is same as the \( I_CQ \) in order to match the diode curves and \( V_{BE} \) curves of the transistor. \( I_CQ \) should be 1 to 5 percent of collector saturation current \( I_{Csat} \).

Average current \( I_{Csat} = V_{CEQ}/\pi R_L = 3/\pi R_L = 43 \, mA \)

\[ I_CQ = I_D = I_{Csat} \times 5\% = 2.15 \, mA \]

Applying KVL in the diode bias network, \( 6 \, V = I_D \times 2R + 1.2 \, V + I_D \times R_B \)

\( I_D \times R_B \) should be about 2 \( V \) to drive into class-AB.

\( I_D \times R_B = 2 \, V \). From this \( R_B = 930 \, \Omega \). Use 1 k.

**Waveforms**
5. Calculate the bandwidth of the amplifier using the expression \( \text{BW} = f_H - f_L \).

**Observation and graph**

<table>
<thead>
<tr>
<th>( f ) in Hz</th>
<th>( V_i ) in Volts</th>
<th>Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\[ V_{\text{in}} = 100 \text{mV} \]

\[ \text{Gain in dB} = -3 \text{ dB} \]

\[ \log f_L \log f_H \]

\[ \log f \]

**Result**  Bandwidth = ····· Hz.

**Answered viva-voce questions**

1. Why is a cascode amplifier called as wide band amplifier?

   The miller capacitance present in ordinary CE amplifier limits the high frequency operation. But in cascode amplifier miller capacitance is absent and hence bandwidth is widened.

2. What are the characteristics of a cascode amplifier?

   \( A_V = \) Same that of CE stage, \( Z_i = \) Same as that of CE stage
   \( A_j = \) Approximately equal to that of CE stage, \( Z_0 = \) Very high like CB stage.

**1.12 RC PHASE SHIFT OSCILLATOR**

**Aim**  To design and set up an RC phase shift oscillator using BJT and to observe the sinusoidal output waveform.

**Components and equipments required**  Transistor, dc source, capacitors, resistors, potentiometer, breadboard and CRO.

**Theory**  An oscillator is an electronic circuit for generating an ac signal voltage with a dc supply as the only input requirement. The frequency of the generated signal is decided by the circuit elements. An oscillator requires an amplifier, a frequency selective network, and a positive feedback from the output to the input. The Barkhausen criterion for sustained oscillation is \( A\beta = 1 \) where \( A \) is the gain of the amplifier and \( \beta \) is the feedback factor. The unity gain means signal is in phase. (If the signal is 180° out of phase, gain will be −1.)
If a common emitter amplifier is used, with a resistive collector load, there is a 180° phase shift between the voltages at the base and the collector. Feedback network between the collector and the base must introduce an additional 180° phase shift at a particular frequency.

In the figure shown, three sections of phase shift networks are used so that each section introduces approximately 60° phase shift at resonant frequency. By analysis, resonant frequency $f$ can be expressed by the equation,

$$f = \frac{1}{2\pi RC \sqrt{\frac{6}{6 + 4\frac{R_c}{R}}}}$$

The three section $RC$ network offers a $\beta$ of 1/29. Hence the gain of the amplifier should be 29. For this, the requirement on the $h_{FE}$ of the transistor is found to be

$$h_{FE} \geq 23 + 29(R/R_C) + 4(R_C/R).$$

The phase shift oscillator is particularly useful in the audio frequency range.

**Circuit diagram**

![Circuit Diagram](image)

**Design**

**Output requirements**  Sine wave with amplitude 10 $V_{PP}$ and frequency 1 kHz.

**Design of the amplifier**  Select transistor BC107. It can provide a gain more than 29 because its minimum $h_{FE}$ is 100.

**DC biasing conditions**  $V_{CC} = 12$ V, $I_C = 2$ mA, $V_{RC} = 40\%$ of $V_{CC} = 4.8$ V, $V_{RE} = 10\%$ of $V_{CC} = 1.2$ V and $V_{CE} = 50\%$ of $V_{CC} = 6$ V.
Waveform

Result Amplitude and frequency of sine wave = \ldots \, \ldots \, V, \, \ldots \, \ldots \, Hz respectively.

Troubleshooting Ensure that the amplifier provides sufficient gain. For this, disconnect the feedback, feed an input sine wave to the amplifier and observe the output. Gain should be more than 33.

Answered examination questions
1. Obtain two sinusoidal signals which are 180° out of phase with each other.
   This can be obtained from an RC phase shift oscillator. Two 180° out of phase signals can be obtained from the base and collector terminals of the transistor. But the amplitude of the signal at base will be small and distorted.

Answered viva-voce questions
1. Classify the sinusoidal oscillators.
   Sinusoidal oscillators can be classified as RC and LC oscillators. LC oscillators are used for high frequency generation while RC oscillators for audio frequency generation.

2. Explain Barkhausen criteria for sustained oscillation.
   a) Total loop gain \((A\beta)\) of the circuit must be exactly unity, where \(A\) is the gain of the amplifier and \(\beta\) is the feedback factor. b) Total phase shift around the loop must be 360°.

3. What are the practical applications of a phase shift oscillator?
   RC-phase shift oscillator is widely used as audio frequency oscillator.

4. What happens when \(C_E\) is removed? Why?
   When \(C_E\) is removed, gain of the amplifier decreases and oscillation gets damped.

5. Why is a minimum \(h_{FE}\) value required for the circuit to function as an oscillator?
   A minimum \(h_{FE}\) is required to obtain sufficient gain for the amplifier part to satisfy the Barkhausen criteria for oscillation.

6. How does one RC section generate a phase difference of 60°?
   Phase shift introduced by one RC network is \(\tan^{-1}(\omega RC)\). Suitable values of \(R\) and \(C\) will provide 60° phase shift between input and output of one RC network at a particular frequency.
1.17 SERIES VOLTAGE REGULATOR WITHOUT FEEDBACK

Aim To study the performance of zener diode regulator with emitter follower output and to plot line regulation and load regulation characteristics.

Components and equipments required Transistor, zener diode, resistor, rheostat, dc source, voltmeter, ammeter and bread board.

Theory The limitations of an ordinary zener diode regulator are, the changes in current flowing through the zener diode cause changes in output voltage, the maximum load current that can be supplied is limited and large amount of power is wasted in zener diode and series resistance.

These defects are rectified in a zener regulator with emitter follower output. It is a circuit that combines a zener regulator and an emitter follower. The dc output voltage of the emitter follower is \( V_o = V_Z - V_{BE} \). When input voltage changes, zener voltage remains the same and so does the output voltage.

In an ordinary zener regulator, if the load current \( I_L \) required is in the order of amperes, zener diode should also have the same current handling capacity. But in zener regulator with emitter follower output, current flowing through the zener is \( I_L/\beta \). Another advantage of this circuit is low output impedance.

The expression for the output voltage can also be expressed as \( V_o = V_i - V_{CE} \). This means that when the input voltage increases, output remains constant by dropping excess voltage across the transistor.

The limitation of this circuit is that the output voltage directly depends on the zener voltage. This is rectified in the series voltage regulator with feedback using error amplifier.

Procedure

1. Set up the circuit on the bread board after identifying the component leads. Verify the circuit using a multimeter.

2. Note down output voltage by varying the input voltage from 0 V to 30 V in steps of 1 V. Plot line regulation characteristics with \( V_i \) along x-axis and \( V_o \) along y-axis. Calculate percentage line regulation using the expression \( \Delta V_o/\Delta V_i \).

3. Keep the input voltage at 15 V and note down output voltage by varying load current from 0 to 500 mA in equal steps using a rheostat. Plot load regulation characteristics with \( I_L \) along x-axis and \( V_o \) along y-axis.
4. Measure the full load voltage $V_{FL}$ by adjusting the rheostat until ammeter reads 500 mA.

5. Remove the rheostat and measure the output voltage to get no-load voltage $V_{NL}$.

6. Mark $V_{NL}$ and $V_{FL}$ on the load regulation characteristics and calculate load regulation as per the equation,

$$V_R = \frac{V_{NL} - V_{FL}}{V_{NL}} \times 100\%$$

**Circuit diagram**

![Circuit diagram](image)

**Design**

Output requirements $V_o = 8.5\ V$, $I_L = 500\ mA$ when input is in the range $15 \pm 5\ V$.

**Selection of transistor** Select the power transistor 2N3055

**Details of 2N3055:** type: Si-NPN. Application: AF Power. Maximum ratings: $V_{CB} = 100\ V$, $V_{CE} = 60\ V$, $V_{BE} = 7\ V$, $I_C\ max = 15\ A$, $P = 115\ W$, Nominal ratings: $V_{CE} = 4\ V$, $I_C = 4\ A$, $h_{FE} = 20$ to 70.

![Top view and pin placement](image)

**Selection of zener diode**

We know that, $V_Z = V_o + V_{BE}$. Since the required output voltage $V_o = 8.5\ V$, $V_Z = V_o + 0.6\ V = 9.1\ V$. Select SZ9.1 zener diode.
Result

Mid-band gain of IF amplifier = ·····
Centre frequency = ····· Hz

1.40 VOLTAGE CONTROLLED OSCILLATOR

Aim To design and set up a voltage controlled oscillator using astable multivibrator for a centre frequency of 1 kHz.

Equipments and components required Transistors, resistors, capacitors, signal generator, bread board and dc supply.

Theory VCO is an oscillator whose frequency can be varied in accordance with an input voltage. It is possible to convert an astable multivibrator into a VCO by connecting an additional voltage source $V_{BB}$ to $R_1$ and $R_2$. The collector supply remains $V_{CC}$. If $V_{BB}$ is varied, the time period of output $T$ changes in accordance with the equation $T = 2RC\ln(1 + V_{CC}/V_{BB})$. With a fixed value of $V_{CC}$, it can be seen from the equation that the output frequency of the circuit is nonlinear function of $V_{BB}$. However, this relation can be linearized by employing a constant current source for linear charging of the capacitor. This circuit is used as an FM generator because frequency of a signal is varied according to the amplitude of another signal.

Circuit diagram
Design

Choose transistor BC107 as $Q_1$ and $Q_2$. For the design of astable part, refer astable multivibrator experiment.

**DC conditions** $V_{CC} = 10$ V and $I_C = 2$ mA. Let $V_{in}$ be 2 V.

**Design of $R_E$** Voltage across $R_E = V_{in} - 2V_{BE} = 2$ V-1.2 V = 0.8 V.

Base current through $Q_1$ or $Q_2$ is $I_B = I_C/h_{FE} = 2$ mA/100 = 20 $\mu$A

To ensure saturation, take base current = 2$I_B$. Then $R_E < V_{RE}/I_B = 0.8$ V/40 $\mu$A = 20 k. Use 22 k std.

Use 2N869 or equivalent as $Q_3$ and $Q_4$

Data of 2N869:

- Maximum ratings: $V_{CB} = 25$ V, $V_{CE} = 18$ V, $V_{EB} = 5$ V, $I_C = 100$ mA
- Nominal ratings: $V_{CE} = 5$ V, $I_C = 10$ mA, $h_{FE} = 20$ (min)

**Design of $R_1$ and $R_2$** Assume base current $I_B$ of $Q_3$ and $Q_4 = I_C/h_{FE} = 40\mu$A/20 = 2 $\mu$A

Let 10$I_B$ flows through $R_1$ and 9$I_B$ through $R_2$

A +5 V at the base of $Q_3$ and $Q_4$ will ensure that their collector base junctions get reverse biased to function as a $CB$ amplifier.

Then $R_1 = 5V/10I_B = 250$ k. Use 220 k std. $R_2 = 5V/9I_B = 278$ k. Use 270 k.

Graph

<table>
<thead>
<tr>
<th>Vin Volts</th>
<th>f in Hz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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</tr>
</tbody>
</table>

| ![Graph](image-url) |

**Procedure**

1. Set up a conventional astable multivibrator using base resistors 82 k. Observe the collector and base waveforms of both transistors.
2. If the astable multivibrator is found to be working properly, connect the remaining components.
3. Feed a 5 V, 10 Hz sine wave as the input $V_{in}$. Observe the input and output waveforms on CRO.
4. Replace the sine wave by a 5 V dc. Vary the dc voltage and note down the corresponding frequency. Enter it in tabular column and draw the graph with dc voltage along x-axis and frequency along y-axis.

**Waveforms**

![Waveforms Diagram](image-url)